IC chip with alternate wiring modes

Publication number: DE19922186 (C1)
Publication date: 2000-10-19
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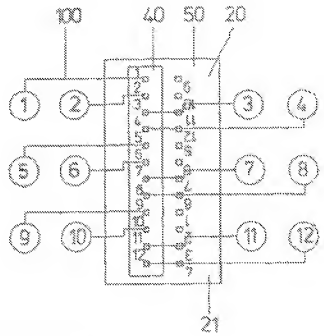
Classification:
- international: ***H01L21/60; H01L23/50;*** **H01L21/02; H01L23/48;** (IPC1-7): H01L23/50
- European: H01L23/50
Application number: DE19991022186 19990512
Priority number(s): DE19991022186 19990512

Also published as:
JP2002544672 (T)
WO0068995 (A1)
US2002060372 (A1)

Cited documents:
DE19756529 (A1)
US5903443 (A)
US5502621 (A)

Abstract of **DE 19922186 (C1)**

The IC chip (20) has a number of terminals provided by at least two groups of metal terminal pads (1-12) , positioned on the upper side or underside of the IC chip, the first group of terminals used for a standard pin layout connections and the second group of terminals used for mirror-image pin layout connections. The IC chip is positioned in two alternate orientations for connection in a standard pin layout or a mirror-image pin layout, e.g. by rotating it about an axis perpendicular to its upper and lower surfaces.



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The invention relates to a IC chip in accordance with preamble of the claim 1. Such a IC chip already is from the US-PS 5.502.621 known.

IC chips, thus integrated semiconductor circuits ("IC" stands for "Integrated Circuit"), become nowadays used in the most different applications. Usually they are high-more complex more electrical part and/or. electronic circuits. These circuits become frequent on circuit boards and/or. Boards realized, which become with or several such IC chips equipped and are on those in or several layers conductor tracks applied, those the single IC chips with one another and/or. connect with other electrical or electronic components. Usually the IC chips exhibits metallic pads, which are connected over wire connections ("bonds") to the conductor tracks and which are a certain predetermined electrical functionality assigned in each case ("pin allocation" or "pin Assignment"). To the protection before destruction the IC chips are generally lived. Beside the classical type of the connection of the IC chips, soldered with which the bond Drähtchen becomes by the board passed and on the backside with the associated conductor track, nowadays also different connection techniques become as for example in or reciprocal Surface Mounted the Technology ("SMT") used connected with which the IC chips with their bonds become direct with the conductor tracks, on the same side of the board are as the IC chips with the assembly of boards. In addition, when this assembling and/or. Assembly technology are if necessary. Connections by the board through or, with use of multi-layer layers of conductor tracks, from a wiring layer to another wiring layer possible by corresponding bores ("via bores") in the board and/or. in the respective layers. To the realization same conductive strip-prolonged ("channel lengths") z. B. with the reciprocal assembly of boards with a plurality of same IC chips and/or. to the avoidance and/or. Reduction disturbing line crossovers ("Crossover") and/or. undesirable prolonged capacities and - it proved inductances with parallel to each other longitudinal conductor tracks ("CROSS talc") as convenient to use with the assembly of several similar IC chips on a board beside IC housings with a standard wiring also IC housings with a so called Mirror image wiring. With this type of the wiring the electrical functionality of the IC chip obtained remains, the wiring in the comparison to the standard wiring however around central axis is reflected a realized.

A known example of this type, how it is in US 5.903.443 and the there described state of the art disclosed, is in the Fig. 1 to 3 shown. With this solution a chip 20 provided on its top 21 is with (square) metallic pads ("Pads") 1 to 12, the one certain pin allocation suggested by the numbering exhibits and with the wiring the 100 (Fig. 1), 102 (Fig. 2) and/or. 101 (Fig. 3) a Interposers

▲ top

connected are. The wiring 100, 101, 102 exhibits terminals ("ball") at their free ends, which are in each case a number 1 to 12 associated, which corresponds in each case to that of the associated Anschlussfleckens 1 to 12. The pin allocation of the single pads 1 to 12 on the top 21 of the IC chip 20 corresponds thus to the precise pin allocation of the corresponding terminals 1 to 12 the interpos he wiring 100, 101, 102. The wiring is so designed that the free terminals 1 to 12 are in pairs 20 arranged on the left and on the right apart from the IC chip. The arrangement of the terminals 1 to 12 in Fig. 1 shows a standard wiring and/or. Standard pin allocation with the pin allocations 1, 2, 5, 6, 9, 10 on side of the IC chip 20 and the pin allocations 3, 4, 7, 8, 11, 12 on the opposite side of the IC chip 20. The arrangement of the terminals 1 to 12 in the Fig. 2 and 3 shows against it a Mirror imagewiring in each case and/or. Mirror image pin allocation, those in relation to the standard pin allocation in accordance with Fig. 1 to the central axis of the IC chip 20 is reflected, which runs parallel to the series of the pads 1 to 12 on the top 21 of the IC chip 20. The embodiment in Fig. the Fig differs 2 from that. by the fact 3 that in Fig. 2 the layout of the IC chip 20 with the layout of the chip 20 in Fig. 1 agrees and the wiring layout of the Interposers 102 in Fig. 2 opposite the wiring layout 100 in Fig. 1 changed is, during in Fig. 3 the wiring layout 101 of the Interposers with the wiring layout 100 of the Interposers in accordance with Fig. 1 agrees, during here the chip layout and/or. the pin allocation of the pads 1 to 12 in Fig. 2 (sequence in Fig. 2 from top to bottom: 4, 3, 2, 1, 8, 7, 6, 5, 12, 11, 10, 9) opposite the chip layout and/or. the pin allocation of the pads 1 to 12 in Fig. 1 (sequence in Fig. 1 from top to bottom: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12) changed is. Disadvantage of this known solution is that the IC chips 20 in at least two embodiments, i.e. in the standard design (Fig. 1) and at least in corresponding a for this "reflected" Mirror imageembodiment (Fig. 2 and/or. Fig. 3) to be lived must. This the increased costs of the fabrication of such IC chips and makes the assembly more difficult of boards with such IC chips, since with the assembly of the chips severe must be paid attention to the fact that one that in each case "proper" lived chip, D. h. either the chip in standard design or in Mirror imageembodiment selects.

The IC chip of the US-PS initially specified 5,502,621 avoids these disadvantages. With this chip arranged in a square housing a part of the lateral electrical connections with their associated pin allocation, up-led at the housing, is double performed, such that the terminals with the same pin allocation are arranged mirror-image concerning one both central axis of the square formed chip package located in the chip plane to each other. Central axis are parallel aligned to the outer edges of the chip package. This positioning of the double pin allocation possible it to use the chip without change of the chip layout both in standard design and in Mirror imageembodiment; (lived) the chip is, with other words, depending upon type of the assembly and positioning on the board, either "standard" - chip or for this corresponding "Mirror image" - chip. With chips of this type it is possible, with in and/or. to realize reciprocal assembly of boards geometric very simple structured circuit superstructures; z. B. Chip pairs, who are on the top of the board, against each other over 180 degree twisted, with one another connected and become by corresponding chip pairs on the underside of the board supplemented, whereby the two chip pairs are connected with one another by via bores. The internal construction of the lived IC chip, in particular the internal terminal of the actual integrated semiconductor circuit in the housing to the lateral electrical connections up-led from the housing is in the US-PS 5.502.621 not disclosed.

An other possibility to the realization of "Mirror image" - chip is in the DE 197 56 529 A1 disclosed. The association of the pin allocation becomes a selected by an internal electronic switch.

The object of the invention consists of creating an other IC chip that initially mentioned type which can become mounted without change of the chip layout both in the standard design as well as in the Mirror imageembodiment.

The solution according to invention of the object is shown by the features of the claim 1. The remaining claims contain favourable out and developments of the invention (claims 2 to 11) as

well as a prefered application of the invention (claim 12).

That the invention underlying thought consists of the fact that the IC chip exhibits at least two groups of metallic pads, which are arranged on the top or underside of the IC chip, whereby the first group of pads the standard wiring and/or. the standard pin allocation associated at least and a second group of pads corresponding the for this Mirror imagewiring is and/or. Mirror image pinoccupancy associated is.

A significant advantage of this solution consists of the fact that depending upon geometric positioning and/or. Alignment of the IC chip in the electrical or electronic circuit (z. B. on a board) the chip alternatively in itself a standard wiring resultant from the pin allocation of the selected group of pads or in for this a corresponding and itself from the pin allocation of the other selected group of pads resultant Mirror image wiring mounted will can, without for this the layout of the chip must become changed.

In a first prefered embodiment of the invention become

a) the standard wiring and/or. Standard pin allocation by the positioning of the chip in a first position and
b) the Mirror imagewiring and/or. Mirror image pinoccupancy by the positioning of the chip in a second position realized. With this solution the two positions of the chip are so constituted that the second position is transferable by rotation of the chip around a vertical to the upper or underside of the chip aligned axis (and reverse).

The angle of rotation knows relative to each other on the chip z depending upon spatial arrangement of the two groups of pads. B. 90 DEG or 270 DEG or, preferably, 180 DEG amount to.

In a second prefered embodiment of the invention become

a) the standard wiring and/or. Standard pin allocation by the positioning of the chip in a first position and
b) the Mirror imagewiring and/or. Mirror image pinoccupancy by the positioning of the chip in a second position realized. With this solution the two positions of the chip are so constituted that the second position is transferable longitudinal first straight one by translation of the chip along a parallel to the upper or underside of the chip (and reverse).

The advantage of these two embodiments (rotation or translation solution) consists of the fact that by a simple rotation or displacement of the chip relative to the electrical and/or. electronic circuit either the standard design of the wiring and/or. Pin allocation or their Mirror image embodiment realized will can. A change of the chip layout is not required. With the assembly of such chips on boards by Interposern and the the same interpos he type can become both for the standard design as well as for the Mirror imageembodiment used, D. h. also the layout of the Interposers does not have to become changed.

In the following the invention becomes more near explained on the basis the figs. Show:

Fig. 1 a IC chip from above with a wiring in standard design (state of the art);

Fig. 2 a IC chip from above with one to the IC chip in accordance with Fig. 1 corresponding wiring in Mirror image embodiment (state of the art);

Fig. 3 another IC chip from above with one to the IC chip in accordance with Fig. 1 corresponding wiring in Mirror imageembodiment (state of the art);

Fig. 4 a favourable first embodiment of the IC chip according to invention from above with a wiring in standard design;

Fig. 5 the IC chip in accordance with Fig. 4 with a wiring in Mirror imageembodiment;

Fig. 6 a favourable second embodiment of the IC chip according to invention from above with a wiring in standard design;

Fig. 7 the IC chip in accordance with Fig. 6 with a wiring in Mirror imageembodiment;

Fig. 8 a favourable third embodiment of the IC chip according to invention from above with a wiring in standard design;

Fig. 9 the IC chip in accordance with Fig. 8 with a wiring in Mirror imageembodiment.

Into the Fig. 1 to 3 IC chip shown are already known. They show, like other already above described, in each case the top 21 of a IC chip 20 on which metallic pads are 1 to 12 in series arranged, those in each case with the wiring 100 and/or. 101 and/or. 102 of a Interposers connected is. The numbering of the pads 1 to 12 stands. For their pin allocation and its correspondence in the identical numbering of the terminals 1 to 12 at the free ends of the wiring 100 finds and/or. 101 and/or. 102 of the respective Interposers. The wiring 100 in Fig. 1 represents a standard design, while the wiring 101 in accordance with Fig. 3 and 102 in accordance with Fig. 2 various Mirror imageembodiments to this standard design represent. In the comparison for standard design in Fig. 1 became in Fig. 2 the layout of the Interposers changed with unchanged layout of the actual IC chip, during in Fig. 3 the layout of the IC chip changed became (see. the sequence in the pin allocation of the pads 1 to 12 on the IC chip 20 in Fig. 1 and Fig. 3) with unchanged layout of the Interposers.

The Fig. 4 and 5 shows both the same IC chip 20, once with a wiring 100 in standard design (Fig. 4) and once in the corresponding Mirror image embodiment 101 (Fig. 5).

The IC chip 20 exhibits 21 two groups 40 and 50 of metallic pads 1 to 12 on its top, which are in two next to each other located series arranged. The two series lie on two second straight ones, which run parallel to each other and parallel to two of the four outer edges of the rectangular formed IC chip 20. The pads 1 to 12 have all within series the equal distance to the direct in each case adjacent pads. The pads 1 to 12 of both series lie in pairs on fourth straight ones, which run vertical to the two second straight ones, and have all - under the parallelism of the two second straight ones - the equal distance. The numbering, D. h. Pin allocation of the single pads 1 to 12 corresponds to the first group 40 of the numbering of the pads 1 to 12 of the IC chip 20 in the case in accordance with Fig. 1 (standard design: 1, 2, . . , 12), while the numbering, D. h. Pin allocation of the single pads of the second group 50 of the numbering of the pads 1 to 12 of the IC chip 20 in accordance with Fig. 3 (Mirror imageembodiment: opposite for the numbering of the first group 40 corresponds to 4, 3, 2, 1, 8, 7, 6, 5, 12, 11, 10, 9) and beyond that also in the series runs.

The Mirror imageembodiment in accordance with Fig. 5 realized becomes, by the IC chip 20 to the interpos he wiring 100 in accordance with Fig, relative on the basis of its first position. 4, around the central axis vertical to the top 21 of the IC chip 20 to the interpos he wiring 101 in accordance with Fig, relative around 180 degree into its second position. 5 rotated becomes. In the same way the Mirror imageembodiment can in accordance with Fig. 5 by rotation around 180 degree around mentioned central axis into the standard design in accordance with Fig. 4 transfered become.

The Fig. 6 and 7 shows both the same IC chip 20, once with a wiring 100 in standard design (Fig. 6) and once in the corresponding Mirror image embodiment 101 (Fig. 7). The difference to the IC chip 20 in accordance with the Fig. it consists 4 and 5 of the fact that with the IC chip 20 in accordance with Fig. 6 and 7 the numbering in both groups 60 (standard design) and 70 (Mirror imageembodiment) of the pads 1 to 12 in both series in the same direction, D. h. here

(exemplarily) from top to bottom runs.

The Mirror imageembodiment in accordance with Fig. 7 realized becomes, by the IC chip 20 to the interpos he wiring 100 in accordance with Fig, relative on the basis of its first position. 6, on a straight one parallel to the top 21 of the IC chip 20 and parallel to the fourth straight ones, D. h. transverse to the two series of pads 1 to 12 to the interpos he wiring 101 in accordance with Fig, relative into its second position. 7 shifted becomes. In the same way the Mirror imageembodiment can in accordance with Fig. 7 by displacement along the mentioned straight ones into opposite direction into the standard design in accordance with Fig. 6 transfered become.

The Fig. 8 and 9 shows both the same IC chip 20, once with a wiring 100 in standard design (Fig. 8) and once in the corresponding Mirror image embodiment 101 (Fig. 9). The difference to the IC chips 20 in accordance with the Fig. 4 and 5 and/or. it consists 6 and 7 of the fact that with the IC chip 20 in accordance with Fig. 8 and 9 the two groups 80 (standard design) and 90 (Mirror imageembodiment) of the pads 1 to 12 in common series summarized is, which lie on a third straight one. In this common series belong the pads 1 to 12 alternate either the one or to the other one of the two groups 80 and 90, D. h. the single numbers of the standard pin allocation 1, 2, 3. . . 12 and those the Mirror image pin allocation 4, 3, 2, 1, 8, 7, 6, 5, 12, 11, 10, 9 is here into one another toothed and 12 summarized to a common numbering 4, 1, 3, 2, 2, 3, 1, 4, 8, 5, 7, 6, 6, 7, 5, 8, 12, 9, 11, 10, 10, 11, 9. The numbering made also here in the same direction, D. h. from top to bottom.

The Mirror imageembodiment in accordance with Fig. 9 realized becomes, by the IC chip 20 to the interpos he wiring 100 in accordance with Fig, relative on the basis of its first position. 8, on a straight one parallel to the top 21 of the IC chip 20 and kolinear to the third straight one, D. h. kolinear to the common series of the pads 1 to 12 (dual number) to the interpos he wiring 101 in accordance with Fig, relative into its second position. 9 shifted becomes. In the same way the Mirror image embodiment can in accordance with Fig. 9 by displacement along the mentioned straight ones into opposite direction into the standard design in accordance with Fig. 8 transfered become.

A significant advantage of these three execution variants of the IC chip according to invention consists of the fact that both for the standard design (Fig. 4; Fig. 6; Fig. 8) the wiring as also for the corresponding Mirror imageembodiment (Fig. 5; Fig. 7; Fig. 9) only in each case a layout of the IC chip per execution variant as well as (common) a layout of the interpos he wiring for all variants required become.

An other advantage consists of the fact that by simple assembly measures (rotation of the chip around 180 degree and/or. Transla< DP N=13> tion the chip crosswise or lengthwise to the series of the pads) the standard design into the Mirror imageembodiment of the wiring transfered will can and reverse.

The invention is not on the represented embodiments limited, but rather on other more transferable.

Like that it is z. B. possible, in place of the arrangement of the pads on straight one other linienförmige arrangements such as z. B. Half or quarter circles, zigzag lines, arc etc. or other laminar geometric arrangements such as circles, triangles, four and other polygons etc. to select; it must be only ensured ones that the required pads on the upper or underside of the chip are to an at least dual present (in standard and in Mirror imageembodiment) and that on the other hand the selected arrangements of the pads the rotation and/or. translation-symmetrical requirements with placing these arrangements of pads on the upper and/or. Underside of the chip fulfill. In case of required rotational symmetry the pads z can. B. on a common circle with the axis of rotation as center lie. The pads group (standard design) can lie thereby on one of the two halves of the circle and the pads of the other group (Mirror image embodiment) on the other half. , Similar is in

addition, more conceivable to the solution in accordance with Fig. 8 and 9 that the pads on the circle become evenly distributed and alternate arranged derived from both groups, so that required to the transfer of the standard design of the wiring into the corresponding Mirror imageembodiment of the wiring only a rotation is around 360 Grad/n, whereby n is the number of pads of a group.

Furthermore it is possible, the vertical electrical occupancy, D. h. to configure the vertical position by a metal-fixed or by fuses ("Fuses") corresponding. The significant advantage of such a solution consists of the fact that only a masque in the FE must become changed and that the number of the pads (and thus the space requirement) is smaller than with the doubling of the pads in accordance with the solution variants in Fig. 4 to 9.

Reference symbol list
1 number of a Anschlussfleckens and/or. Wiring ball
2 number of a Anschlussfleckens and/or. Wiring ball
3 number of a Anschlussfleckens and/or. Wiring ball
4 number of a Anschlussfleckens and/or. Wiring ball
5 number of a Anschlussfleckens and/or. Wiring ball
6 number of a Anschlussfleckens and/or. Wiring ball
7 number of a Anschlussfleckens and/or. Wiring ball
8 number of a Anschlussfleckens and/or. Wiring ball
9 number of a Anschlussfleckens and/or. Wiring ball
10 number of a Anschlussfleckens and/or. Wiring ball
11 number of a Anschlussfleckens and/or. Wiring ball
12 number of a Anschlussfleckens and/or. Wiring ball
20 IC chip
21 top of the IC chip
30 group of pads (state of the art)
40 first group of pads (invention)
50 second group of pads (invention)
60 first group of pads (invention)
70 second group of pads (invention)
80 first group of pads (invention)
90 second group of pads (invention)
100 standard wiring layout
101 Mirror image wiringlayout
102 other Mirror image wiringlayout

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1. IC chip, with several connection devices, which are in each case a certain predetermined pin allocation associated, which pin allocation is multiple present, whereby the IC chip can itself be mounted likewise alternatively in a standard wiring resultant from the pin allocation or in one from the pin allocation resultant and to the standard wiring reflected Mirror imagewiring, characterised in that as connection devices at least two groups (40, 50; 60, 70; 80, 90) of metallic pads (1-12) provided is, which are arranged on the top (21) or underside of the IC chip (20); that the first group (40; 60; 80) from pads (1-12) the standard wiring or standard pin allocation associated is and at least a second group (50; 70; 90) from pads (1-12) corresponding the for this Mirror imagewiring or Mirror image pinoccupancy associated is.

2. IC chip according to claim 1, characterised in that with predetermined standard wiring layout (100) and Mirror image wiringlayout (101) the standard wiring or standard pin allocation by the positioning of the IC chip (20) in a first position realized is that the Mirror imagewiring or Mirror image pinoccupancy is by the positioning of the IC chip (20) in a second position realized and that the second position is transferable by rotation of the IC chip (20) around a vertical to the top (21) or underside of the IC chip (20) aligned axis or by translation of the IC chip (20) along a parallel to the top (21) or underside of the IC chip (20) longitudinal first straight ones into the first position (and reverse).

3. IC chip according to claim 2, characterised in that to the transfer of the second position in the first position and reverse in each case a rotation around 90 DEG or around 270 DEG or preferably around 180 DEG required is.

4. IC chip after one of the claims 2 or 3, characterised in that the standard wiring (100) and corresponding the for this Mirror imagewiring (101; 102) itself in each case on two itself opposite sides of the IC chip (20) over the IC chip (20) outside extended.

5. IC chip after one of the preceding claims, characterised in that the first group (40; 60; 80) of pads (1-12) in first series and the second group (50; 70; 90) from pads (1-12) in second series arranged are or that the pads (1-12) of both groups (40, 50; 60, 70; 80, 90) alternate in common series arranged is.

6. IC chip according to claim 5, characterised in that the first and second series next to each other arranged are.

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7. IC chip after one of the claims 5 or 6, characterised in that the single pads (1-12) of the first

series and the single pads (1-12) of the second series within its own series in each case the equal distance to their direct adjacent pads of its own in each case group (40, 50; 60, 70; 80, 90) has or that the single pads (1-12) of the group (40; 60; 80) in the common series in each case the equal distance to their direct adjacent pads (1-12) that in each case different group (50; 70; 90) have.

8. And the pads (1-12) of the second series on parallel longitudinal second straight ones are appropriate for IC chip after one of the claims 5 to 7, characterised in that the pads (1-12) of the first series to each other or that the pads (1-12) for the common series on a third straight one are appropriate.

9. Direct opposite pads (1-12) first and the second series on a fourth straight one are appropriate themselves for IC chip according to claim 8, characterised in that in each case, which run vertical to the two second straight ones.

10. IC chip after one of the claims 5 to 9, characterised in that the pin allocation of the pads (1-12) of the first group (40; 60; 80) along the first series or along the common series against-intimate (40, 50) or in the same direction (60, 70; 80, 90) is for the pin allocation of the pads (1-12) of the second group (50; 70; 90).

11. IC chip after one of the claims 5 to 10, characterised in that to the transfer of the second position of the IC chip (20) in the first position and reverse in each case a translation transverse to the first and second series or in each case a translation along the common series required is.

12. IC chip after one of the preceding claims, characterized by the use as IC chip to in or reciprocal assembly of boards by means of SMT.